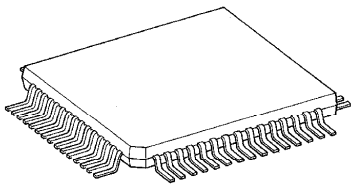
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T9947S, JT9947X-AS

T9947S, JT9947X-AS CMOS 1 CHIP LSI FOR LCD ELECTRONIC CALCULATOR

The T9947S, JT9947X-AS is a 1 chip microcomputer for 10-digits 1-memory electronic calculator.
T9947S, JT9947X-AS can drive the liquid crystal display (LCD). Single power supply operation, low power consumption make it suitable for solar battery or battery operated pocketable calculator.



LQFP60-P-1414-0.80

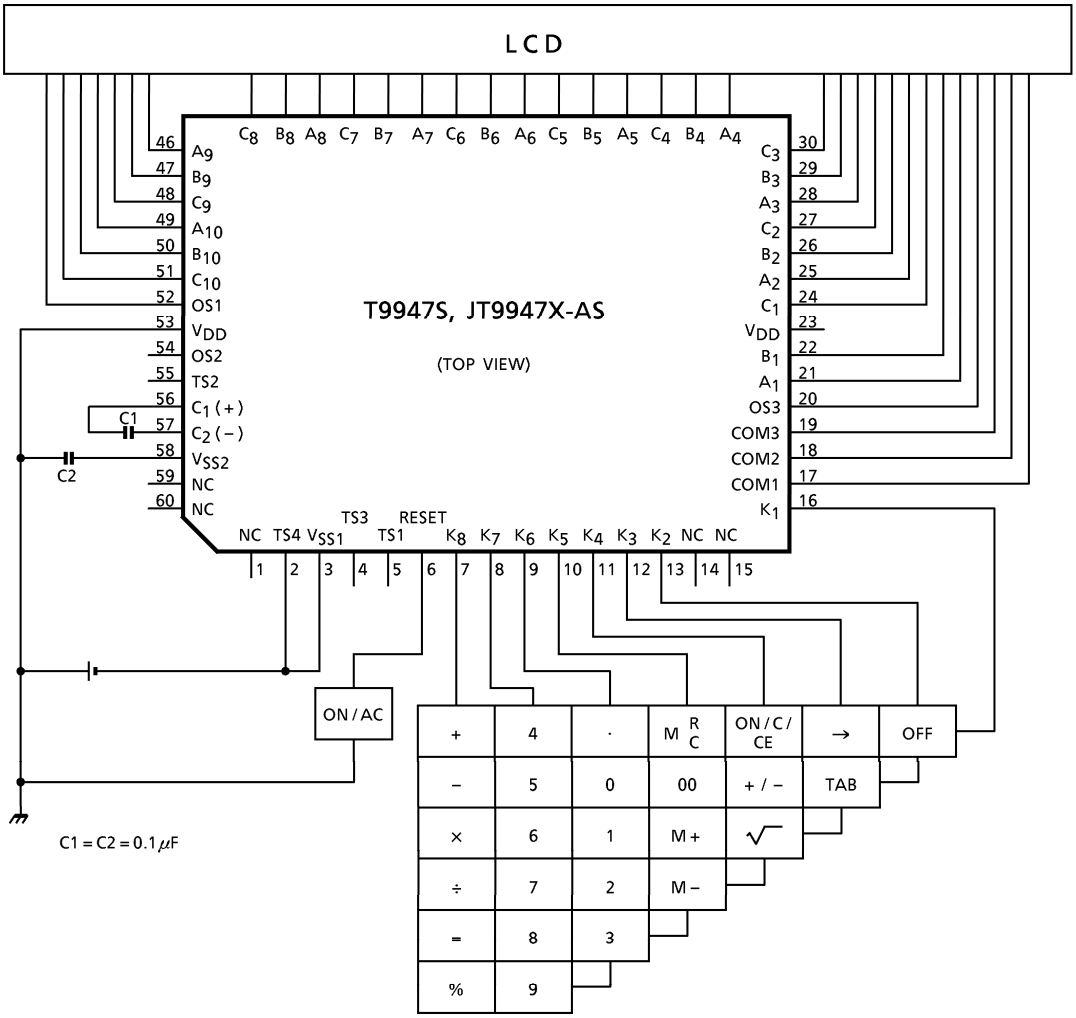
Weight : 0.66g (Typ.)

FEATURES

- 10 digits of data and 1 symbol digit for calculator.
- Algebraic calculation mode.
- Punctuation.
- Standard 4 functions (+, −, ×, ÷), square root, percent with automatic add-on / discount, automatic constant calculations, chain calculations, memory calculations with memory overflow protection.
- Internal keyboard decoding and denouncing.
- Complementary output buffer for direct driving of liquid crystal display (LCD : FEM type −3.0V, 1/2 bias, 1/3 duty).
- Single power supply (−1.5V typ.).
- Quad in line flat package (60 PIN).
- Very low power consumption (3.0μW typ. at wait).
- Very wide range of operating voltage (V_{SS1} = −1.2~ −2.0V).

SYSTEM BLOCK DIAGRAM

Battery Type

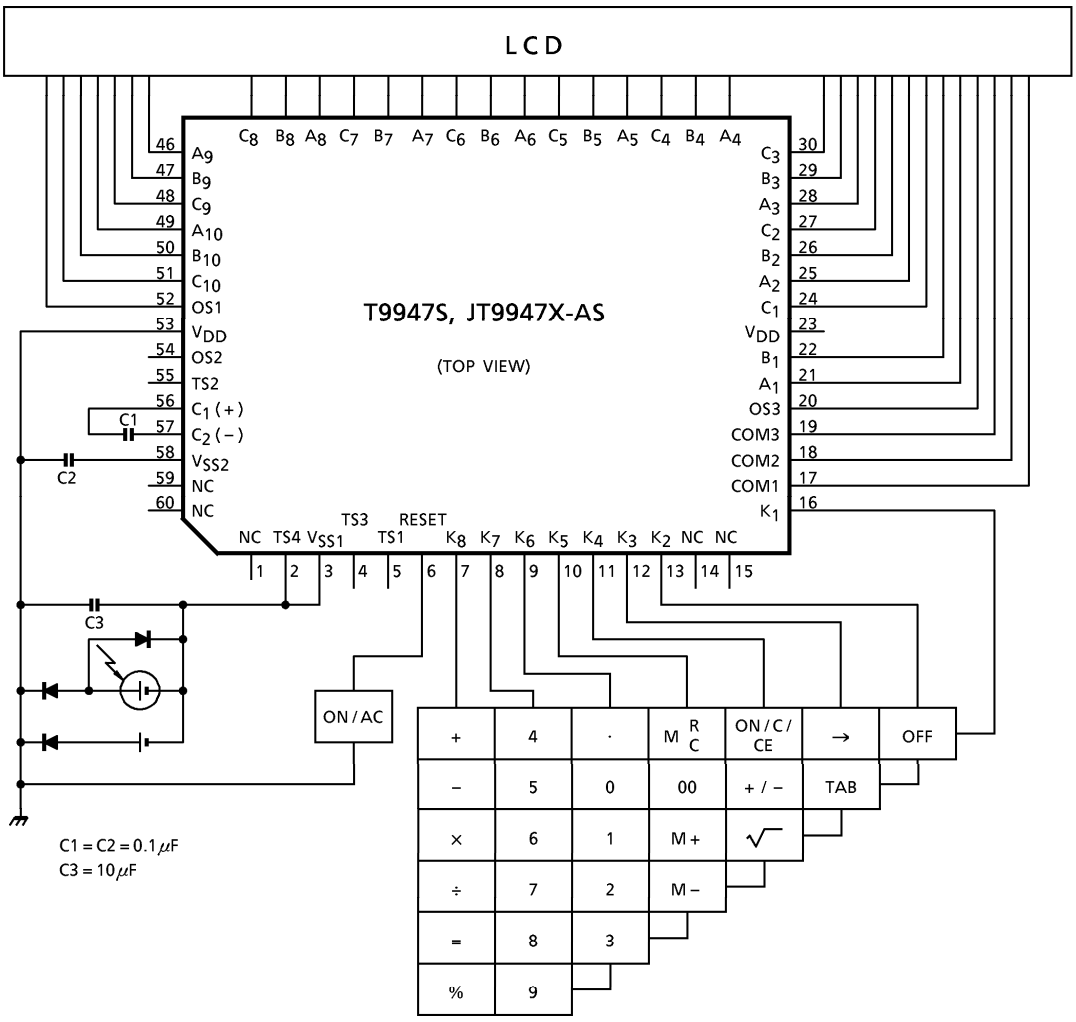


[NOTE]

TS4 { V_{DD} ……OFF MODE DISABLE
V_{SS1} ……OFF MODE ENABLE

Rkey ≦ 20kΩ (– 1.2V)
≦ 135kΩ (– 1.5V)

Dual Type

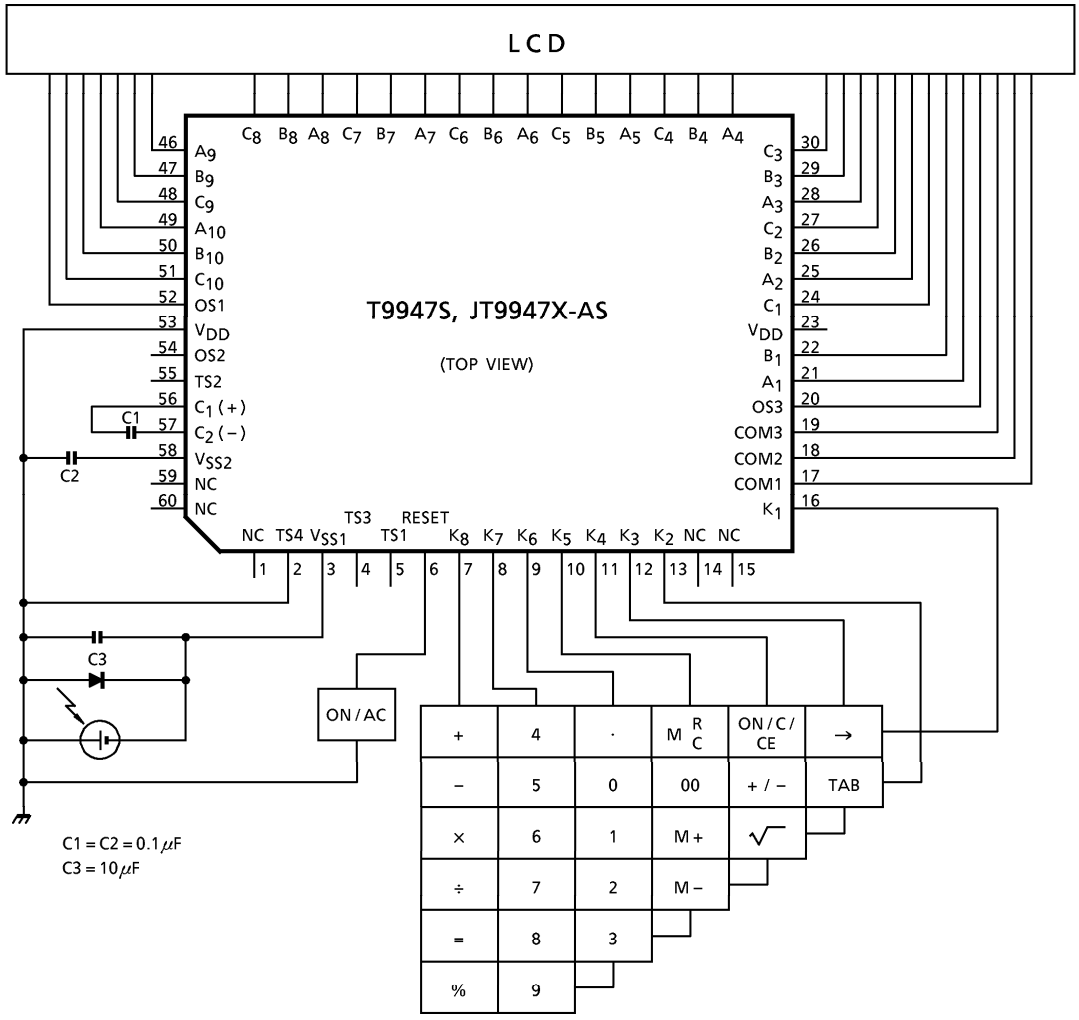


[NOTE]

TS4 { V_{DD} ……OFF MODE DISABLE
V_{SS1} ……OFF MODE ENABLE

Rkey ≦ 20kΩ (– 1.2V)
≦ 135kΩ (– 1.5V)

Solar Type



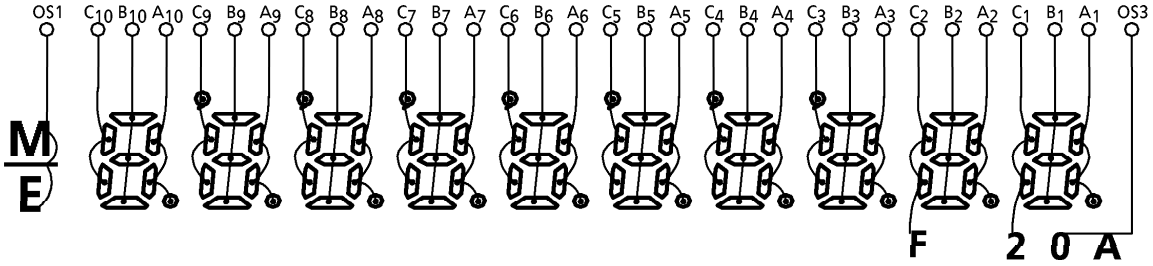
[NOTE]

TS4 { V_{DD} ……OFF MODE DISABLE
V_{SS1} ……OFF MODE ENABLE

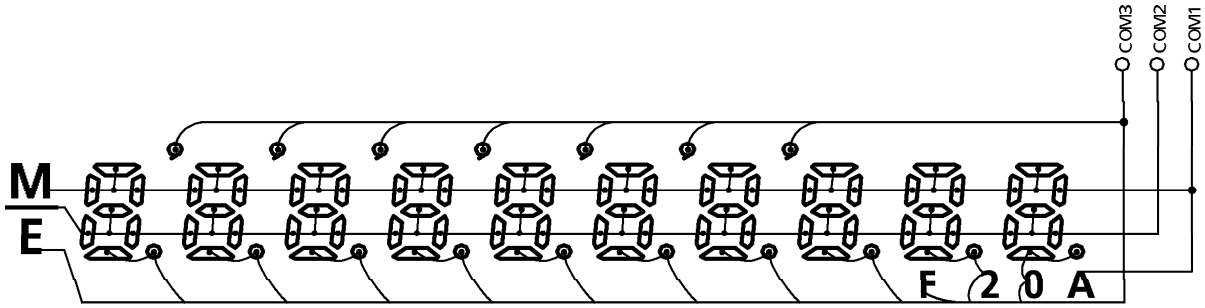
Rkey ≦ 20kΩ (− 1.2V)
≦ 135kΩ (− 1.5V)

CONNECTION OF LCD

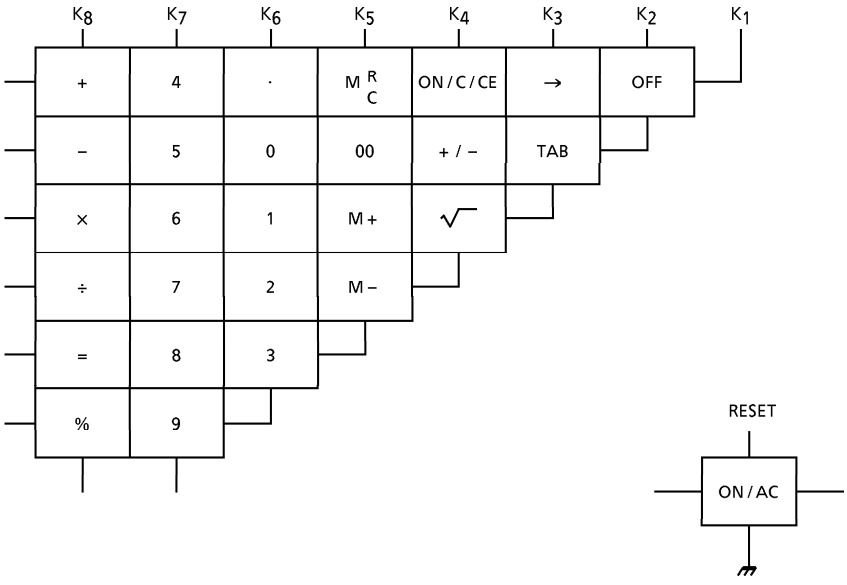
SEGMENT



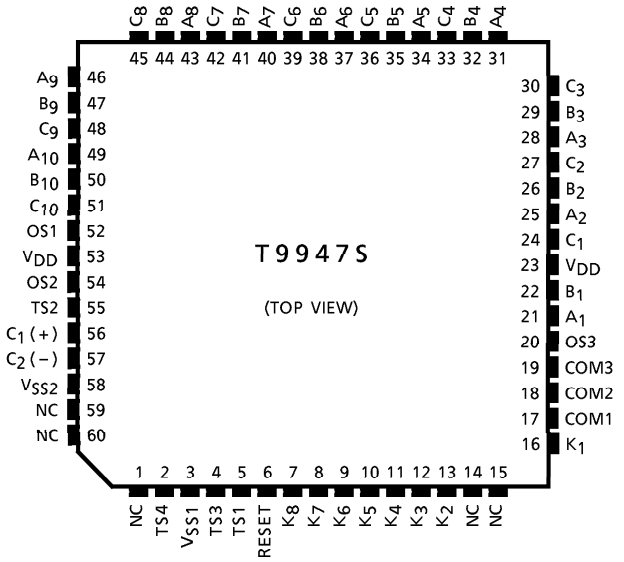
COMMON



KEY LAYOUT



PIN LAYOUT



SPECIFICATION OF CALCULATOR

Operational Features

(1) 10 digits of data and 1 symbol digit.

(2) Algebraic mode.

(3) Full floating point.

(4) Standard 4 functions +, −, ×, ÷.

(5) Memory calculation.

(6) Square root.

(7) Percent with automatic add-on and discount.

(8) Constant calculation (Automatic constant).

(9) Chain calculation.

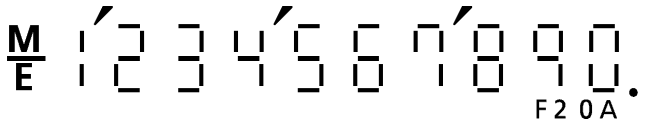
(10) Leading zero suppression.

(11) Trailing zero suppression.

Capacity of Calculation

(1)	Numeral entry	10 digits
(2)	Addition / Subtraction	10 digits + (−) 10 digits = 10 digits
(3)	Multiplication / Division	10 digits × (÷) 10 digits = 10 digits
(4)	Memory calculation	10 digits + (−) 10 digits = 10 digits
(5)	Square root	$\sqrt{10}$ digits = 10 digits

Display Font



Overflow Condition

(1) When division by zero is attempted, an overflow condition will result, and error symbol "E" and a zero are displayed.

(2) When the integer part of result exceeds 10 digits, the display will show 10 most significant digits of result divided by 10^{+10} and "E".

(3) When the integer part of result exceeds 19 digits, display will show a zero and "E".

(4) When the integer part of result in memory register exceeds 10 digits at memory calculation, display will show a zero and "E", and previous data will be kept in memory resister.

(5) When an overflow occurs on the way of add-on / discount calculation, display will show a zero and "E".

(6) When square root of any negative number is attempted, "E" and square root of absolute value are displayed.

(7) In overflow condition, any operation or numeral entry will be inhibited.

Clearing Overflow Condition

(1) The resulting overflow condition can be cleared by depressing [ON / C / CE] .

(2) At memory overflow condition, depression of [$\frac{MR}{C}$] after [ON / C / CE] will recall the previous memory data.

(3) At the condition of exceeding capacity overflow occurred in chain calculation, depression of [ON / C / CE] will reset the error symbol "E", and you can continue the calculation using the displayed data.

Speed of Calculation

(1)	Numeral entry					74.4ms
(2)	Addition	1111111111	+	1111111111	=	102.7ms
(3)	Multiplication	1	×	9999999999	=	394.7ms
(4)	Division	9999999999	÷	1	=	394.7ms
(5)	Memory calculation	9999999999	÷	1	M+	482.7ms
(6)	Percentage calculation	1	+	9999999999	%	378.7ms
(7)	Square root			9999999999	√	326.7ms

Keys for Calculator

(1) Data Keys

The data keys consist of numeral keys 0 , 00 through 9 and a decimal point key · . The first of a sequence of data keys will clear the contents of display register before being entered. The decimal point key will be accepted the first time it is depressed during calculations.

(2) Arithmetic Operation Keys

The arithmetic operation keys include the plus + , minus − , multiply × , divide ÷ , equal = , percent % , square root √ , memory add M+ , memory subtract M− , sign change +/− , data shift →.

+ Depression of this key conditions the calculator for addition of display register to upper register.
If the calculator was previously conditioned for add, subtract, multiply or device, those operation would be performed with the resultant intermediate sum, difference, product or quotient displayed and previous modes and reset, and calculator stores add command.
In the successive depressions of this key, the first will perform the previously enabled mode and more than twice depressions will be ignored.

− Depression of this key performs the same function as the + key with the exception that calculator stores subtract mode.

× Depression of this key conditions the calculator for multiplication of upper register and display register.
If the calculator was previously conditioned for add, subtract multiply or divide, those operation would be performed with the resultant intermediate sum, difference, product or quotient displayed.
And then set the multiply mode.

M − Depression of this key will perform the same function as the M + with the exception that the calculator result or displayed number is subtracted from the memory register.

= Depression of this key following numeral entry will perform the previously enabled mode.
If no number has been entered, the displayed number will be used to perform the previously enabled mode. If no mode are enabled, this key will be ignored. If multiplication or division are enabled, constant mode operations are performed by termination a sequence of operations with the = key, entering a new number and depressing the = key.
Any key sequence terminated with, = key will not require the use of ON / C / CE key before a new operation sequence can be initiated.

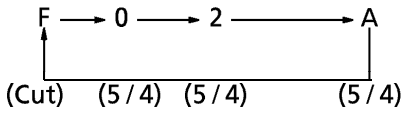
% If the calculator was previously conditioned for addition, or subtraction or multiplication or divination, % calculations would be performed as follows.

a + b % a + a·b / 100
a − b % a − a·b / 100
a × b % a·b / 100
a ÷ b % 100 a / b

If no mode are enabled, this key will be ignored. If multiplication or division are enabled, constant mode operations are performed by terminating a sequence of operation with the % key, entering new number and depressing the % key.

M + Depression of this key will perform the previously enabled mode and add the result to memory register and leave the result in the display register.
If no modes are enabled, the displayed number is added to memory register by this key.
Any key sequence terminated with M + will not require the use of the ON·/ C / CE key before a new operation sequence can be initiated.

TAB "TAB" fixed point mode selectable



÷ Depression of this key performs a similar function as the × key except that division of upper register by display register is either set up or performed and the divide mode is activated.

[√] Depression of this key calculated the square root of number displayed without changing modes of operation.
Depression of this key following [+], [−], [×], or [÷] keys will transfer the contents of display register to upper register and calculate the square root of number displayed.
The entry of a new number following this key clear the previous display.

[+ / −] Depression of this key will change the sign of display register.

[→] Depression of this key will shift the right data of display register.

(3) Command Function Keys

The command function keys include the clear entry / clear all [ON / C / CE] , recall / clear memory [MRC]

[MRC] Depression of this key following [+], [−], [×] or [÷] will transfer the contents of display register to upper register and recall the contents of memory register to display register.
[MRC] key following [=] , [%], [M+], [M−] or any number key will recall the contents of memory register to the display register without affecting any other operations in progress.
Successive depressions of [MRC] key will clear the memory register.

[ON / C / CE] Depression of this key after [MRC], [√] , [·], or numeral keys will clear the display register.
You can reset the error symbol "E" if you depress [ON / C / CE] at the condition of exceeding capacity error.

[OFF] Depression of this key will off the LSI.

Arithmetic Operations

1. Addition

Key Op.	Display
A	A
[+]	A
B	B
[+]	A + B
C	C
[=]	A + B + C
D	D
[+]	D
E	E

		Key Op.	Display
		[+]	D + E
		[=]	D + E

2. Subtraction

	(1)	A	A
		[−]	A
		B	B
		[−]	A − B
		C	C
		[=]	A − B − C
		[−]	A − B − C
		D	D
		[+ / −]	− D
		[−]	A − B − D + D
		[=]	− (A − B − C + D)

3. Multiplication

	(1)	A	A
		[×]	A
		B	B
		[=]	A·B
		[+]	A·B
		C	C
		[=]	A·B + C
	(2)	[−]	0.
		A	A
		[×]	− A
		B	B
		[=]	− A·B

		Key Op.	Display
4. Division			
	(1)	A	A
		[÷]	A
		B	B
		[=]	A / B
	(2)	[−]	0.
		A	A
		[÷]	− A
		B	B
		[=]	− A / B
5. Power calculation			
	(1)	A	A
		[×]	A
		[=]	A^2
		[=]	A^3
	(2)	A	A
		[÷]	A
		[=]	1 / A
		[=]	$1 / A^2$
	(3)	[−]	0.
		A	A
		[×]	− A
		[=]	A^2
		[=]	$- A^3$
	(4)	[−]	0.
		A	A
		[÷]	− A
		[=]	− 1 / A
		[=]	$1 / A^2$

	Key Op.	Display
(5)	A	A
	×	A
	=	A^2
	×	A^2
	=	A^4

6. Mixed calculation

(1)	A	A
	×	A
	B	B
	+	A·B
	C	C
	÷	A·B + C
	D	D
	−	$\frac{A \cdot B + C}{D}$
	E	E
	=	$\frac{A \cdot B + C}{D} - E$

7. Constant calculation

(1)	A	A
	×	A
	B	B
	=	A·B
	C	C
	=	A·C
(2)	−	0.
	A	A
	×	− A
	B	B
	=	− A·B
	C	C

	Key Op.	Display
	[=]	– A·C
(3)	A	A
	[÷]	A
	B	B
	[=]	A / B
	C	C
	[=]	C / B
	D	D
	[×]	D
	[=]	D^2
(4)	A	A
	[+]	A
	B	B
	[=]	A + B
	C	C
	[=]	C
(5)	A	A
	[−]	A
	B	B
	[=]	A – B
	C	C
	[=]	C
(6)	A	A
	[×]	A
	B	B
	[=]	A·B
	C	C
	[×]	C
	D	D

	Key Op.	Display
	[=]	C·D
	E	E
	[=]	C·E
	[×]	C·E
	F	F
	[=]	C·E·F
	G	G
	[÷]	G
	H	H
	[=]	G / H
	I	I
	[=]	I / H
(7)	A	A
	[×]	A
	B	B
	[%]	A·B / 100
	C	C
	[%]	A·C / 100
	D	D
	[÷]	D
	E	E
	[%]	100·D / E
	F	F
	[%]	100·F / E

8. Mark-up / Discount calculator

(1)	A	A
	[×]	A
	B	B
	[+]	A·B
	[=]	A + A·B

	Key Op.	Display
(2)	A	A
	×	A
	B	B
	−	A·B
	=	A − A·B
(3)	A	A
	×	A
	B	B
	%	A·B / 100
	+	A·B / 100
	=	A + A·B / 100
(4)	A	A
	×	A
	B	B
	%	A·B / 100
	−	A·B / 100
	=	A − A·B / 100
(5)	A	A
	+	A
	B	B
	%	A + A·B / 100
(6)	A	A
	−	A
	B	B
	%	A − A·B / 100

9. Memory calculation

	Key Op.	Display	Memory
(1)	A	A	0.
	M +	A (M)	A
	B	B (M)	A

	Key Op.	Display	Memory
	[M+]	B (M)	A + B
	C	C (M)	APB
	[M–]	C (M)	A + B – C
	D	D (M)	A + B – C
	[MRC]	A + B – C (M)	A + B – C
	MRC	A + B – C	0.
(2)	A	A	0.
	[+]	A	0.
	B	B	0.
	[M+]	A + B (M)	A + B
	[+]	A + B (M)	A + B
	[M+]	A + B (M)	2 (A + B)
	C	C (M)	2 (A + B)
	[M–]	C (M)	2 (A + B) – C
(3)	A	A	0.
	[×]	A	0.
	B	B	0.
	[M+]	A·B (M)	A·B
	C	C (M)	A·B
	[×]	C (M)	A·B
	D	D (M)	A·B
	[M–]	C·D (M)	A·B – C·D
	[MRC]	A·B – D·D (M)	A·B – C·D
	[M–]	A·B – C·D	0.
(4)	A	A	0.
	[×]	A	0.
	B	B	0.
	[=]	A·B	0.
	C	C	0.
	[M+]	C (M)	C

	Key Op.	Display	Memory
	[=]	A·C (M)	C
	D	D (M)	C
	[M −]	D (M)	C − D
	[=]	A·D (M)	C − D
(5)	A	A	0.
	[M +]	A (M)	A
	B	B (M)	A
	[M +]	B (M)	A + B
	[MRC]	A + B (M)	A + B
	×	A + B (M)	A + B
	[MRC]	A + B (M)	A + B
	[+]	$(A + B)^2$ (M)	A + B
	C	C (M)	A + B
	[=]	$(A + B)^2 + C$ (M)	A + B
(6)	1.000000001	1.000000001	0.
	M +	1.000000001 (M)	1.000000001
	9999999999	9999999999. (M)	1.000000001
	[M +]	0. (M_E)	1.000000001
	[ON / C / CE]	0. (M)	1.000000001
	[MRC]	1.000000001 (M)	1.000000001

10.Square root

(1)	A	A	
	[√]	$\sqrt{A}$	
	B	B	
(2)	A	A	
	[×]	A	
	B	B	
	[√]	$\sqrt{B}$	
	[=]	$A\sqrt{B}$	

	Key Op.	Display	Memory
(3)	A	A	
	[×]	A	
	[√]	$\sqrt{A}$	
	B	B	
	[=]	A·B	
(4)	[−]	0.	
	A	A	
	[=]	− A	
	[√]	$\sqrt{A}$ (E)	
(5)	A	A	0.
	[M+]	A (M)	A
	[MRC]	A (M)	A
	[÷]	A (M)	A
	B	B (M)	A
	[+/−]	− B (M)	A
	[√]	$\sqrt{B}$ ($\frac{M}{E}$)	A
	[ON/C/CE]	0. (M)	A

11. Percentage calculation

(1)	A	A	
	[×]	A	
	B	B	
	[%]	A·B / 100	
	C	C	
	[%]	A·C / 100	
	D	D	
	[%]	A·D / 100	
(2)	A	A	
	[%]	A	
	B	B	

	Key Op.	Display	Memory
	[%]	B	
	C	C	
	[%]	C	
(3)	A	A	
	[−]	A	
	B	B	
	[%]	$A - A \cdot B / 100$	
	[−]	$A - A \cdot B / 100$	
	[+]	$A - A \cdot B / 100$	
	C	C	
	[%]	$\left(A - \frac{A \cdot B}{100}\right) + \frac{\left(A - \frac{A \cdot B}{100}\right) \cdot C}{100}$	

12. Key correction

(1)	A	A	0.
	[×]	A	0.
	[÷]	A	0.
	[−]	A	0.
	[+]	A	0.
	[√]	$\sqrt{A}$	0.
	[M+]	$A + \sqrt{A}$ (M)	$A + \sqrt{A}$
	[+/−]	$-(A + \sqrt{A})$ (M)	$A + \sqrt{A}$
	[MRC]	$A + \sqrt{A}$ (M)	$A + \sqrt{A}$
	[MRC]	$A + \sqrt{A}$	0.
	B	B	0.
	[+]	B	0.
	[−]	B	0.
	[×]	B	0.
	[÷]	B	0.
	[=]	1 / B	0.

13. Others		Key Op.	Display	Memory
	(1)	A	A	
		[+]	A	
		[=]	A	
	(2)	A	A	
		[×]	A	
		[÷]	A	
		[=]	1 / A	
	(3)	A	A	
		[%]	A	
		[+]	A	
		[=]	A	
	(4)	A	A	
		[×]	A	
		[−]	A	
		[=]	− A	
	(5)	A	A	
		[÷]	A	
		[−]	A	
		[=]	− A	
	(6)	A	A	
		[×]	A	
		[ON / C / CE]	0.	
		B	B	
		[=]	B	
	(7)	A	A	
		[×]	A	
		B	B	
		[ON / C / CE]	0.	
		C	C	
		[=]	A·C	

Key Chattering Protection

(1) At time of key on : about 18.0ms, after key input. ($f\phi$ typ.)

(2) At time of key off : about 17.0ms, after completion of the operation ($f\phi$ typ.)

(3) Simultaneous Keying protection

If 2 or more keys are pressed simultaneously, any key input is not accepted.

MAXIMUM RATINGS

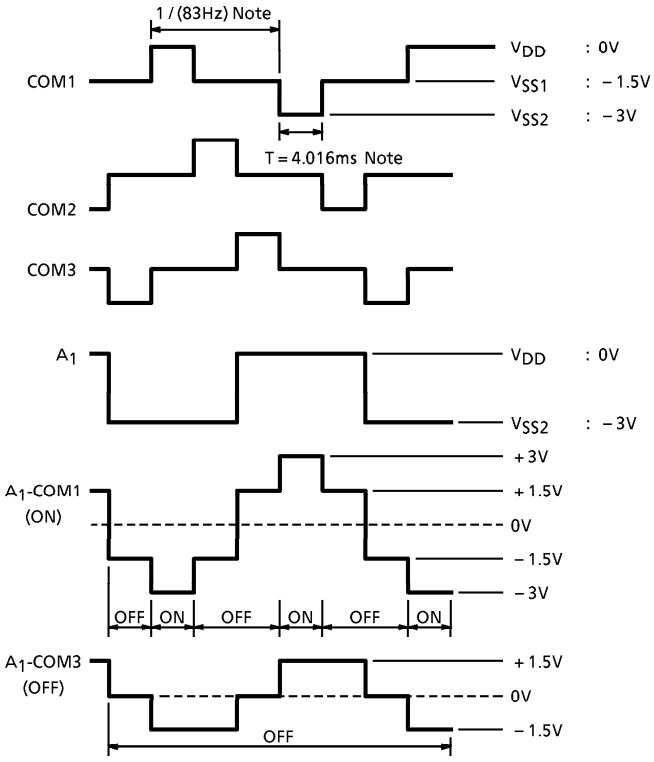
PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{SS1}	+0.3~−2.2	V
Input Voltage	V_{IN}	+0.3~V_{DD1}−0.3	V
Operating Temperature	T_{opr}	+0.0~40	°C
Storage Temperature	T_{stg}	−55~125	°C

ELECTRICAL CHARACTERISTICS (V_{SS1} = −1.5V±0.2V, V_{SS2} = −3.0V±4.0V, V_{DD} = 0V, Ta = 25°C)

PARAMETER		SYMBOL	TEST CIR-CUIT	PIN NAME	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage		V_{SS1}	—	—	—	−1.2	−1.5	−2.0	V
VOLTAGE	Input "1"	V_{IH}	—	K_2~K_8, RESET	—	V_{SS1} +0.4	—	V_{SS1}	V
	Input "0"	V_{IL}	—	K_2~K_8, RESET	—	0	—	−0.4	V
	Output "1"	V_{OH}	—	Segment, Common	—	V_{SS2} +0.2	—	V_{SS2}	V
	Output "0"	V_{OL}	—	Segment, Common	—	0	—	−0.2	V
	Output "1"	V_{OH}	—	K_1~K_8, RESET	—	V_{SS1} +0.2	—	V_{SS1}	V
	Output "0"	V_{OL}	—	K_1~K_6, RESET	—	0	—	−0.2	V
Resistance	Output "1"	R_{OH}	—	Segment	V_{OUT} = V_{SS2} + 0.5V	—	—	70	kΩ
	Output "0"	R_{OL}	—	Segment	V_{OUT} = −0.5V	—	—	70	kΩ
	Output "1"	R_{OH}	—	Common	V_{OUT} = V_{SS2} + 0.5V	—	—	70	kΩ
	Output "0"	R_{OL}	—	Common	V_{OUT} = −0.5V	—	—	70	kΩ
	Pull Up	R_{KH}	—	K_1~K_8	V_{OUT} = 0V	60	400	1500	kΩ
		RESET	—	RESET	V_{OUT} = 0V	180	300	420	kΩ
	Output "0"	R_{OL}	—	K_1~K_6	V_{OUT} = −0.5V	—	—	10	kΩ
Supply Current 1 (On Display)		I_{DD1}	—	—	V_{SS1} = −1.5V (No Keys)	—	−2.2	−3.6	μA
Supply Current 2 (Operation)		I_{DD2}	—	—	V_{SS1} = −1.2V (Peak OF A11 9√‾)	—	−4.4	−6.6	μA
Supply Current 3 (Off)		I_{DD3}	—	—	V_{SS1} = −1.5V (Off Status)	—	−0.5	−2.0	μA
Oscillating Frequency		f_{osc} (WAIT)	—	—	V_{SS1} = −1.5V, On Display	5.4	9	12.6	kHz
		f_{osc} (OP)			V_{SS1} = −1.5V, On Operating	10.8	18	25.2	kHz
Frame Frequency		f_F	—	—	V_{SS1} = −1.5V (Wait)	50	83	117	Hz

WAVEFORMS FOR DISPLAY

Display Device : FEM type LCD −3.0V, 1/2 bias, 1/3 duty dynamic system



Note : $f\phi$ = 9kHz

OTHERS

- AUTO POWER OFF (Typ.) = 7MIN
- RESET Key

  i) After releasing this key, the cpu is reset and display "0".

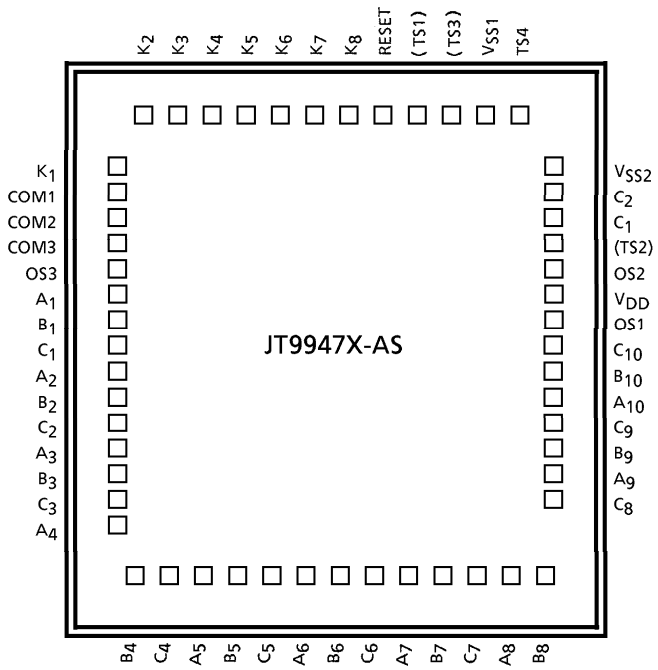
PAD LOCATION TABLE (μm)

No.	NAME	X POINT	Y POINT
1	K_1	– 1291	1093
2	COM1	– 1291	896
3	COM2	– 1291	744
4	COM3	– 1291	592
5	OS3	– 1291	441
6	A_1	– 1291	289
7	B_1	– 1291	137
8	C_1	– 1291	– 14
9	A_2	– 1291	– 166
10	B_2	– 1291	– 318
11	C_2	– 1291	– 470
12	A_3	– 1291	– 621
13	B_3	– 1291	– 773
14	C_3	– 1291	– 925
15	A_4	– 1291	– 1076
16	B_4	– 927	– 1249
17	C_4	– 776	– 1249
18	A_5	– 624	– 1249
19	B_5	– 472	– 1249
20	C_5	– 320	– 1249
21	A_6	– 169	– 1249
22	B_6	– 17	– 1249
23	C_6	135	– 1249
24	A_7	286	– 1249
25	B_7	438	– 1249
26	C_7	590	– 1249
27	A_8	741	– 1249
28	B_8	893	– 1249
29	C_8	1254	– 1077

No.	NAME	X POINT	Y POINT
30	A_9	1254	– 925
31	B_9	1254	– 774
32	C_9	1254	– 622
33	A_{10}	1254	– 470
34	B_{10}	1254	– 319
35	C_{10}	1254	– 167
36	OS1	1254	– 15
37	V_{DD}	1254	137
38	OS2	1254	288
39	*(TS2)	1254	489
40	C_1	1254	697
41	C_2	1254	898
42	V_{SS2}	1254	1100
43	TS4	949	1249
44	V_{SS1}	798	1249
45	*(TS3)	646	1249
46	*(TS1)	494	1249
47	RESET	343	1249
48	K_8	191	1249
49	K_7	39	1249
50	K_6	– 112	1249
51	K_5	– 264	1249
52	K_4	– 416	1249
53	K_3	– 568	1249
54	K_2	– 719	1249

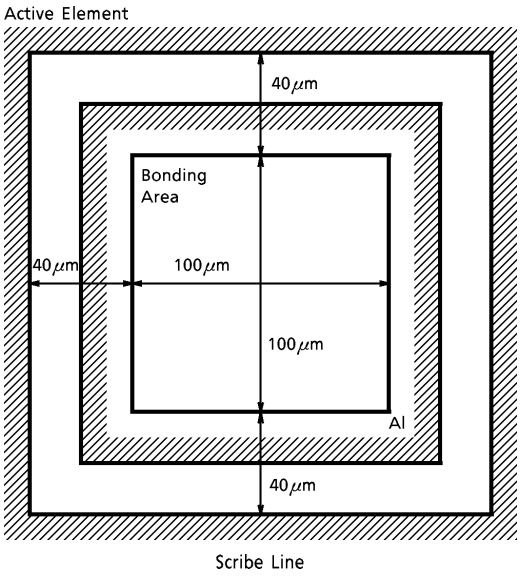
*( ) Do not connect.

CHIP LAYOUT



Chip size : 3.04×3.02 [mm]
Chip thickness : 290±20 [μm]
Substrate : V_{DD}

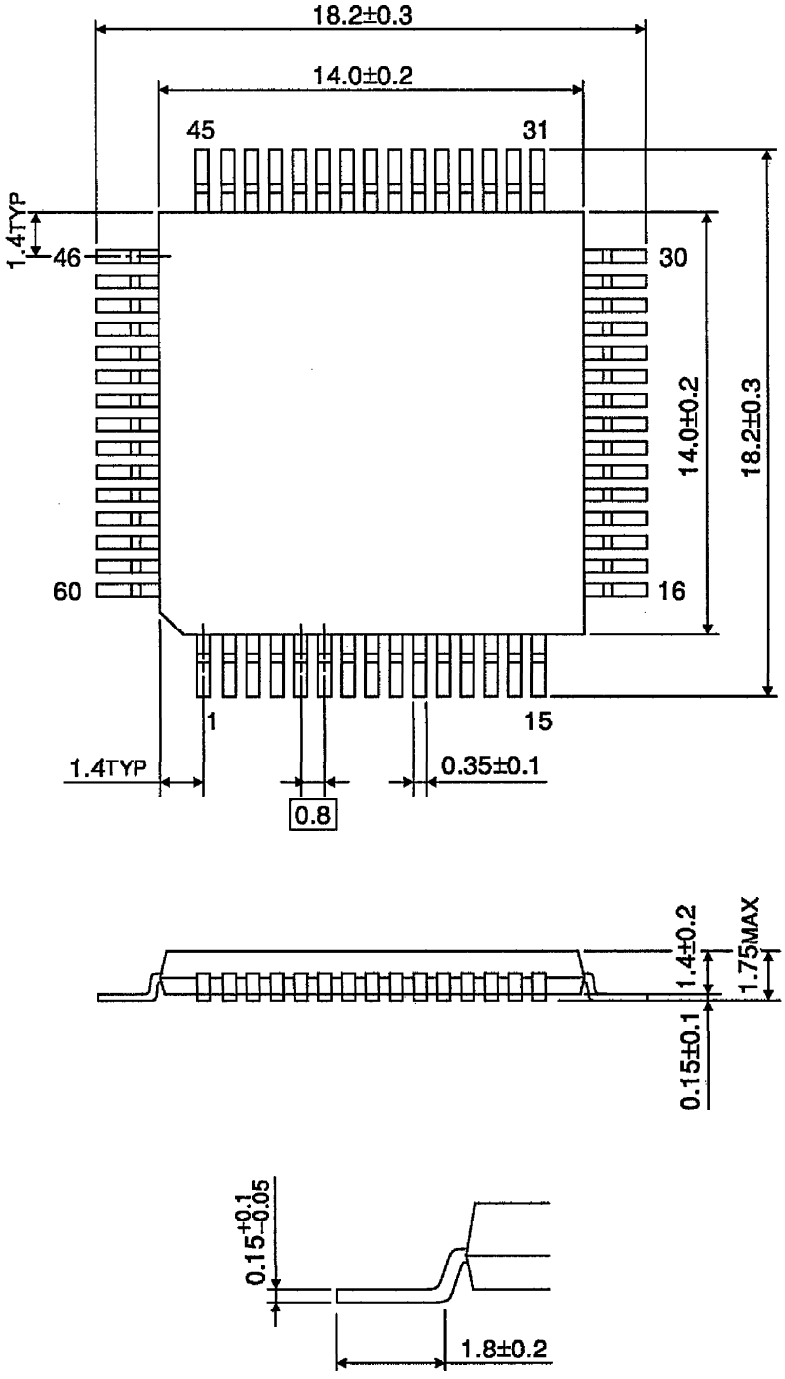
PAD LAYOUT



PAD Pitch 160μm

OUTLINE DRAWING

LQFP60-P-1414-0.80 Unit : mm



Weight : 0.66g (Typ.)

GENERAL SPECIFICATION FOR CALCULATOR LSI BARE CHIP

1. Purpose

   This is to specify the quality standard for the integrated circuit produced by TOSHIBA CORPORATION (hereinafter referred as to VENDOR) to be delivered to PURCHASER.

2. Definition

   This specification applies only to the calculator LSI bare chip produced by VENDOR and purchased by PURCHASER and defined the general specification items.

3. Priority of specifications

   When the discrepancies or questions happen to the specifications and instructions provided by VENDOR, the priority shall be ranked as follows.

   1) Individual specification for the calculator LSI bare chip.
      (Both PURCHASER and VENDOR are confirmed by the special sheets.)
   2) General specifications for the calculator LSI bare chip.
   3) Other related specifications and standards.

4. Characteristics

   To be shown in the individual specification sheets.
   The individual specification shall consist of the following 4 items in principle.

   1) Rated specifications.
   2) Electrical characteristics.
   3) Pin configuration & mechanical dimensions.
   4) Others.

5. Inspection of product for delivery

   5.1 Inspection lot

   a) Inspection lot shall consist of products produced by same material under same design, through same production process, and same facilities and assured same quality by same quality assurance method, and lot number shall be put on all trays to be able to trace the lot history.

   b) The quantity of products per Inspection lot shall consist of all the same VENDOR's lot number.

5.2 Sampling plan

Statistical sampling and inspection shall be in accordance with MIL-STD-105D single sampling plans for normal inspections, general inspection level Ⅱ.

The acceptable quality level (AQL) shall be specified in following table :

TEST ITEM	AQL (%)
Electrical	2.5
Visual	4.0

5.3 Electrical criteria

Criteria of Electrical Characteristics are prescribed in Attachment-1.

5.4 Visual criteria

Visual Criteria are prescribed in Attachment-2.

6. Incoming inspection

6.1 General

a) PURCHASER's incoming inspection should be done within 15 days after PURCHASER receives the quantity of products in principle.

b) PURCHASER shall report the results of incoming inspection to VENDOR and provide VENDOR with detailed data in failure rate and items regarding VENDOR's lot number respectively, if VENDOR demands the report from PURCHASER.

6.2 Inspection procedure

PURCHASER should do his incoming inspection according to the following procedure.

a) First : Visual inspection should be done.

b) Next : Electrical and other inspection should be done under condition with bare chip before going into PURCHASER's process.

7. Treatment for defective lot and products

Regarding the defective lot and defective products which are found through PURCHASER's incoming inspection, PURCHASER can be returned to VENDOR with detailed description on failures concerned.
However, if VENDOR cannot receive the defective items within 30 days after PURCHASER's incoming inspection, VENDOR should be able to make no reference to the defective problem.

8. Packing and labeling

a) Dice shall be placed in die tray with the top metalization facting up in order.

b) In principle, a pile consists of 5 trays and several piles are packed in a package. These piles and packages are indicated with printed labels as shown below.

Date	
Name	
Lot No.	
Net	
TOSHIBA MADE IN JAPAN	

c) PURCHASER shall return these packing materials to VENDOR on VENDOR's demand.

9. Storage criteria

Solid state chips, unlike packaged devices, are non-hermetic devices normally fragile and small in physical size, and therefore, require special handling considerations as follows :

9.1 Chips must be stored under proper conditions to insure that they are not subjected to a moist and / or contaminated atmosphere that alter their electrical, physical, or mechanical characteristics.
After the shipping container is opened, the chips must be stored under the following conditions :

A. Storage temperature, 40°C max.
B. Relative humidity, 50% max.
C. Clean, dust-free environment.

9.2 The user must exercise proper care when handling chips or wafers to prevent even the slightest physical damage to the chip.

9.3 During mounting and lead bounding of chips the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.

9.4 After the chip has been mounted and bounded, any necessary procedure must be followed by the user to insure that these non-hermetic chips are not subjected to moist or contaminated atmosphere which might cause the development of electrical conductive paths across the relatively small insulating surfaces.
In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably adversely affect their proper performance.

10. Handling criteria

The user should find the following suggested precautions helpful in handling chips.
In any event, because of the extremely small size and fragile nature of chips, care should be taken in handling these devices.

10.1 Grounding

a) Bonders, pellet pickup tools, table tops, trim and form tools, sealing equipment, and other equipment used in chip handling should be properly grounded.

b) Operator should be properly grounded.

10.2 In-process handling

a) Assemblies or subassemblies of chips should be transported and stored in conductive carriers.

b) All external leads of the assemblies or subassemblies should be shorted together.

VISUAL INSPECTION CRITERIA

1. Visual inspection magnification shall be 40 × in principle.
2. Defects defined :

2.1 Thickness

See the technical data sheet.

2.2 Chip and crack

A die shall be rejected if :

a) Any crack of chip extends greater than 35μm in length into the inside of the scribble line. (see Fig.1)

2.3 Metallization

A die shall be rejected if :

a) More than 25% of the designed area of the metallization is missing at any bonding pad.

b) There is a short or break which affects electrical characteristics in any lead pattern. (see Fig.2)

2.4 Glass protection coat

A die shall be rejected if :

a) It exhibits glass protection coat which covers more than 25% of any active bonding pad.

2.5 Attached foreign material

A die shall be rejected if :

a) A die is covered by stains or attached foreign material which size is more than 5 times as large as a bonding pad area.

b) It exhibits residual ink, stains or attached foreign material which covers more than 20% of any active bonding pad. (see Fig.3)

2.6 Others

A die shall be rejected if :

a) There have no evident probed impression on the bonding pads.

b) A inked die, defective die, is intermized.

3. Limit samples should be fized, if necessary.

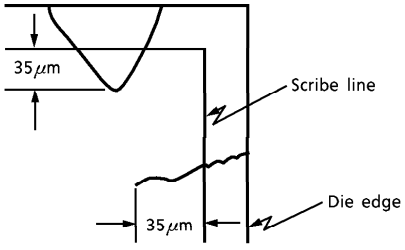


Fig.1

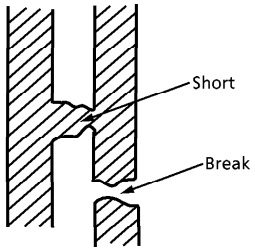


Fig.2 Lead pattern

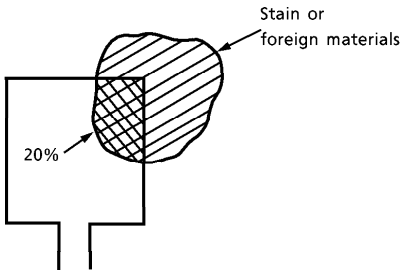
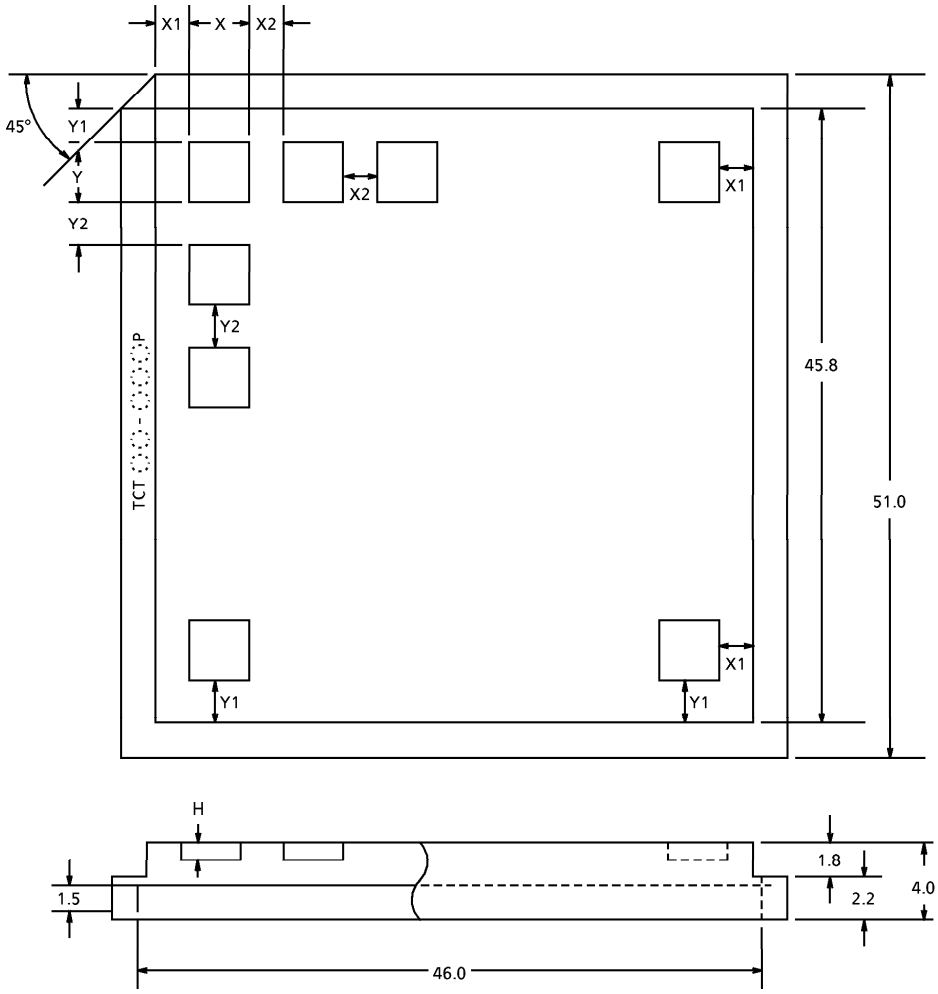


Fig.3

OUTSIDE DIMENSIONS OF CHIP TRAY



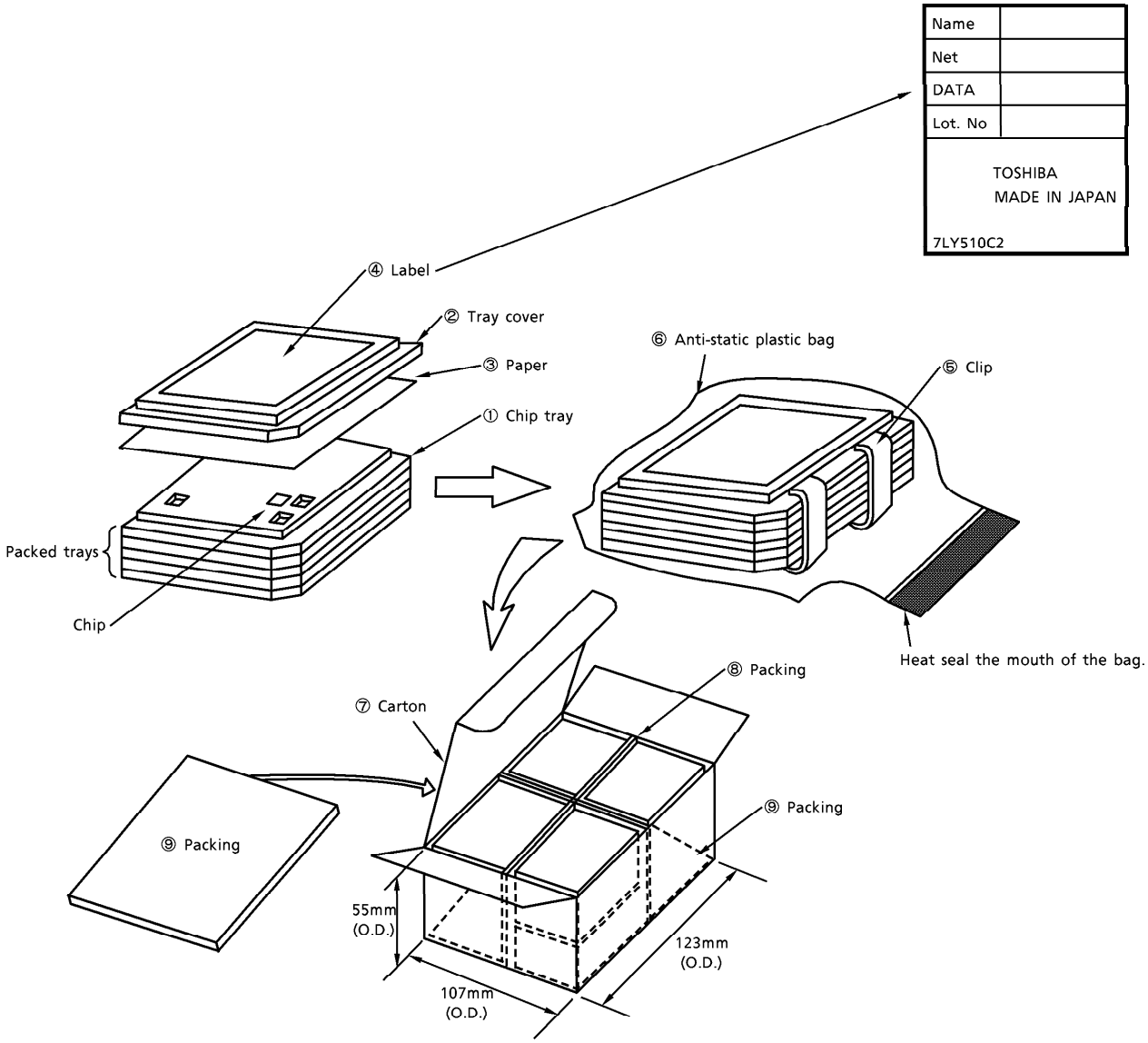
Unit : mm

CHIP NAME	TRAY NAME	X	Y	(H)	No. OF POCKETS	X1	X2	Y1	Y2
JT9947X-AS	TCT33-060P	3.30	3.30	0.60	10 × 10 (100)	1.900	1.000	1.900	1.000

Tray material :

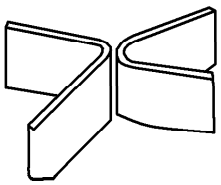
Carbon-containing polypropylene

PACKING METHOD-1



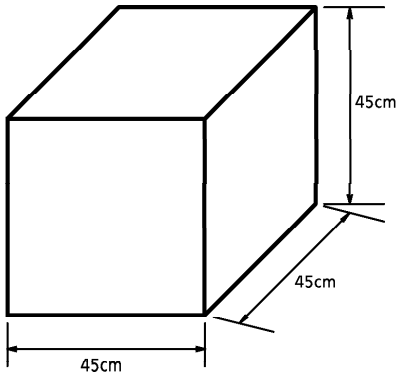
Place eight bags of chip trays in each carton box ⑦. Lay one sheet of packing ⑨ (7UF44F) before closing the lid of the cart box. (See the diagram above.)

Prepare packing ⑧ by cutting 7UF44F into halves and folding each in half as shown below ; use them as inner partitions.



PACKING METHOD-2

Shipping box



- Inner box : Containing 20 boxes
- Weight : Approx. 15kg (including packing material)
- Material : Corrugated cardboard
- IC contents : 36×5×8×20=28.8kpcs.